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(54) Title DATA RECORDING METHOD FOR VTR

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Claims

1. A data recording method for a VTR, characterized by the following facts: a header with a fixed pattern,

an identification signal that is set either immediately after the header or immediately before and immediately after the header and used for identifying the type of a plurality of types of data, such as the position information of a magnetic tape related to video signals recorded/reproduced by a VTR or a comment on the recorded information content, and

digital signals that are set immediately after the identification signal or include the identification signal as part of the data and have a signal format synthesized in time series with one type of data selected arbitrarily out of said plurality of types of data are used as one block; the duty cycle of control pulses with a certain period is varied for the value of each bit of digital signals having said header further added to the last part of only the last block, and the control pulses are recorded on the control track of said magnetic tape.

2. The data recording method for a VTR cited in Claim 1, characterized by the fact that said header is selected and recorded at such a value that the pattern is the same regardless of whether said magnetic tape runs in the forward direction or the backward direction.

Detailed explanation of the invention

Industrial application field

The present invention relates to a data recording method for a VTR. In particular, the present invention relates to a method that records the position information data of a magnetic tape recorded/reproduced by a VTR (magnetic recording/reproducing device), any comment information, or other VTR data on said magnetic tape itself.

Prior art

In the case of editing or randomly accessing a magnetic tape having video signals or audio signals recorded by a VTR, it is necessary to know the position information, particularly, the absolute address of the recorded magnetic tape.

Conventionally, a VTR that forms a special time code track separately from the video signal recording tracks by using a fixed head to record and reproduce SMPTE time code signals determined based on the SMPTE (Society of Motion Picture and Television Engineers) of the United States is known as a VTR that can obtain an absolute address. The aforementioned time code signal is a code signal that determines the tape address in a 24-h system of hour, minute, second, frame with TV frame as the smallest unit. When the time code signal is recorded/reproduced, it is possible to know the absolute address of the magnetic tape with high accuracy.

Also, a VTR that modulates the pulse width of the control pulses by using a time code signal indicating the absolute address, records the modulated control pulses on the control track, and demodulates and separates the time code signal from the control pulses during reproduction to obtain the absolute address of the magnetic tape is known as another VTR that can obtain the absolute address (for example, the VTR described in Japanese Kokai Utility Model Application No. Sho 57[1982]-34633).

On the other hand, the method for recording multiplexed information disclosed in Japanese Kokai Patent Application No. Sho 55[1980]-55406 is known as another conventional technology that switches the duty cycle of the control pulses recorded on the control track of a magnetic tape although the absolute address is not obtained. In addition, Japanese Kokai Patent Application No. Sho 55[1980]-55407 discloses a multiplexed information recording system that divides the rising or falling in one period of the aforementioned control pulse into a plurality of sections and makes the states of the plurality of sections correspond to the signals to multiplex.

Problems to be solved by the invention

For the aforementioned VTR that records and reproduces SMPTE time code signals, however, an SMPTE time code signal comprises an 80-bit bi-phase modulated signal per frame. It has a 64-bit data area and a 16-bit syncword with a fixed pattern used for indicating partitioning of the frame. Since it is a coded signal with a complicated configuration having time code bits and user's bits arranged in a comb form every four bits in the data area, the VTR can be used for a broadcast that is required to have a quite accurate editing function. However, since the time code generator and the time code reader are extremely complicated and expensive, this VTR is unsuitable for use in general households that require a low price.

The aforementioned conventional VTR that modulates the pulse width of the control pulses with a time code signal can be constituted at low cost. However, since the time code signal is recorded automatically on the control transistor at the same time as the video signal, the user cannot record any comment information or address information as desired. This significantly limits its application range.

The aforementioned multiplexed information recording method and the multiplexed information recording system can simply record a plurality of data on the control track compared with the aforementioned method that modulates the pulse width of the control pulses by using a time code signal. However, they can only record the data indicating the type of the multiplexed information (for example, indicating whether the type of the multiplexed audio information is stereo or monaural) but still cannot record any comment information or address information. Therefore, the application range is extremely limited.

The objective of the present invention is to solve the aforementioned problems by providing a data recording method for a VTR that can record a plurality of types of data with very abundant information contents on a control track.

Means to solve the problems

According to the data recording method for a VTR disclosed in the present invention, a header with a fixed pattern, an identification signal used for identifying the type of a plurality of types of data, and digital signals that are set immediately after the identification signal or include the identification signal as part of the data and have a signal format synthesized in time series with one type of data selected arbitrarily out of said plurality of types data are used as one block. The duty cycle of the control pulses with a certain period is varied for the value of each bit of the digital signals having said header further added to the last part of only the last block, and the control pulses are recorded on the control track of said magnetic tape.

Operation

For a plurality of types of data, such as the position information of the magnetic tape used for recording/reproducing video signals by a VTR or a comment on the recorded information content, any type of data can be selected and synthesized in time series immediately after the aforementioned identification signal and recorded along with the header. Alternatively, the aforementioned identification signal can also be recorded along with the header as part of the data. In the latter case, the data type can be identified when the identification signal has a value other than a prescribed value.

The aforementioned arbitrarily selected data are recorded in a block unit on the control track with a varied (modulated) duty cycle of the control pulse. However, for the last block (when there is no other block immediately after that block), the aforementioned header is added and recorded in the last part of that block. Consequently, the header can be reproduced first regardless of whether the magnetic tape is played back in the forward direction or the backward direction.

Also, since the aforementioned header is selected and recorded at such a value that the pattern is the same no matter whether said magnetic tape runs in the forward direction or the backward direction, even during playback in the backward direction, a header with the same pattern as that during the playback in the forward direction can be reproduced.

Application examples

Figure 1 shows an application example of the signal format of each data item recorded by the method of the present invention. The present invention provides a method that appropriately selects a plurality of types of data, varies the duty cycle of the control pulses with a certain period corresponding to the values of the selected data, and records the control pulses on the control track on a magnetic tape. Figures 1(A)-(C) show the signal formats of three types of data.

Figure 1(A) shows the signal format of an application example of the address data. In this figure, each of 1-1 to 1-4 is a 11-bit header with a fixed pattern that is common to each data item. For example, the values of the two bits, that is, the most significant bit (MSB) and the least significant bit (LSB) are "0". The value of each of the nine bits from the second bit to the tenth bit is "1". The signal has the same pattern regardless of if the magnetic tape runs in the forward direction or the backward direction. 4-bit x 4-digit address information data 2-2 to 2-3 are arranged after headers 1-1 to 1-3, respectively.

For each of address information data items 2-1 to 2-3, the value of each digit of "thousand", "hundred", "ten", and "one" is represented by a 4-bit BCD code. Each address information data item has a total of 16 bits. The four bits of the most significant digit, that is, "thousand," are arranged right after the four bits of header 1-1 to 1-3. Its value is in the range of

"0" – "9" but not "10" – "15" as a decimal number (that is, "A" – "F" as a hexadecimal number). When it is detected that the 4-bit value immediately after the header represented by 1-1 to 1-3 is neither hexadecimal number "A" nor "B" of the identification signal to be described later, it can be identified in the reproduction system to be described later that the reproduced data are address information data. In other words, if the 4-bit value immediately after the header of 1-1 to 1-3 is a value other than hexadecimal value "A" or "B", it is also used as the address information data identification signal.

The address information data can be the random data of any address, such as "0100", "0175", "0210", "1500", or "2000", input from a keyboard. It can also be a certain address information having continuity from the beginning end of the tape (such as "0010", "0020", "0030"...).

As described above, the address data are synthesized in time series and are recorded, reproduced in a block unit having 27 bits comprising 11-bit header and 16-bit address information data.

Figure 1(B) shows the signal format of an application example of character (comment) data. In this figure, 3-1 and 3-2 are 11-bit headers with a fixed pattern. Their values are the same as the values of headers 1-1 to 1-4 shown in Figure 1(A). Identification signals 4-2, 4-3 represented by A_H and having a value of "A" as a hexadecimal number are arranged as the 4 bits immediately before and the 4 bits immediately after header 3-2, respectively (same for header 3-1 and other headers). By using these identification signals, it is possible to identify in the reproduction system to be described later that the reproduced data are character data.

Said identification signal 4-1 is set as the 4 bits immediately after header 3-1, followed by a total of 10 6-bit character information data D_0-D_9 and 4-bit identification signal 4-2. Each of said character information data D_0-D_9 only uses part of the ASCII code (for example, 59 characters from space SP to capital character Z). In this way, the 8 bits of the ASCII code are compressed to 6 bits, and the bit rate is smaller than that of the existing ASCII code.

The reason for adding an identification signal not only immediately before headers 3-1 to 3-2 but also as 4 bits, such as 4-2, immediately after the headers is that the character data have a higher bit rate compared with the other two types of data. In this way, the fact that the reproduced data are character data can be immediately identified in the reproduction system not only during fast forwarding but also during rewinding.

As described above, the character data are synthesized in time series and are recorded, reproduced in a 79-bit block unit comprising an 11-bit header, two 4-bit identification signals, and 60-bit (= 6 bits x 10) character information data.

Figure 1(C) shows the signal format of an application example of the special function data. In this figure, headers 5-1 to 5-4 have the same values as those of headers 1-1 to 1-3, 3-1,

3-2 shown in Figures 1(A) and (B), respectively. They are 11-bit signals with a fixed pattern. 4-bit identification signals 6-1 to 6-4 represented by B_H and having hexadecimal value "B" are set as the 4 bits immediately after headers 5-1 to 5-4, respectively. Special function information data 7-1 to 7-3 comprising 3 digits of 4-bit BCD codes are set as the 12 bits after identification signals 6-1 to 6-3. By using said identification signals 6-1to 6-4, it is possible to identify the data as special function data in the reproduction system.

As described above, the special function data are synthesized in time series and are recorded, reproduced in a 27-bit block unit comprising an 11-bit header, 4-bit identification signal, and 12-bit special function information data. The table below shows an example of the 16-bit hexadecimal value comprising the identification signal immediately after the header and the special function information data and the content of the corresponding special function.

Value of the code	Content of the special function
B000	End of recording of video signals, audio signals
B001	Start of skip
B002	End of skip
B003	Header position of video signals, audio signals
B004	Header position of video signals
B005	Header position of audio signals
1	1

In the table shown above, skip is a mode that automatically fast forwards a recording section from the beginning time point to the ending time point without playback. It is used, for example, in the case of skipping playback of a commercial broadcast period (recording period) after TV broadcast signals are recorded.

The aforementioned three types of data are selected appropriately and recorded as desired by the user of the VTR. The present invention is characterized by the fact that the aforementioned plurality of data is recorded in the signal formats shown in Figures 1(A)-(C).

Figures 2(A), (B) show the recording pattern of an application example of the control track recorded by the method of the present invention. Figure 2(A) shows a pattern in which address data 8 have the same repeated content and are recorded three times in the block unit on the control track, followed by recording special function data 9 that have the same repeated content three times in the block unit. Figure 2(B) shows a pattern in which the character data have the same repeated content and are recorded three times in the block unit represented by 10a-

10c on the control track. In Figures 2(A), (B), the hatched parts represent the headers. Also, Ⓐ and Ⓑ represent said identification signals with hexadecimal values "A", "B", respectively.

Also, in Figure 2(B), when no data of a different type or the same type are recorded immediately after last block 10c of the character data, a header represented by 80 is added there as shown in Figure 2(B). In this way, regardless of whether the magnetic tape runs in the forward or backward direction, the data can always be reproduced immediately after the header, making it easy to identify and reproduce the data.

In the following, a recording/reproducing device used for realizing the method of the present invention will be explained. Figure 3 shows the overall configuration of an example of a data recording/reproducing device. As shown in the figure, VTR 11 incorporates one-chip microcomputer (microcomputer) 12, reading/writing circuit 13, and character generator 14. Also, operation part 16 used for recording/reproducing data and character output on/off switch 17 are added to the display panel surface in addition to display part 15. Keyboard 18 is connected to the VTR. Like a normal VTR, VTR 11 also has lid 19 that is opened/closed when loading/unloading a tape cassette.

VTR 11 outputs the reproduced output video signals and audio signals as well as the recorded/reproduced data to monitor TV 21 via cable 20.

Comment screen switch 28 in data recording/reproducing operation part 16 is a switch used for switching the display of screen 29 of monitor TV 21. It is connected in any of the three switch positions, that is, on (ON), off (OFF), and scroll (SCROLL). When it is in the "ON" position, "KEY IN" and "TAPE OUT" are displayed at the bottom on the screen 29 of monitor TV 21. Also, a 10-character key input is displayed on the right side of "KEY IN" in the same line. A 10-character comment reproduced from the control track as to be described later is displayed on the right side of "TAPE OUT" in the same line (this display mode is referred to as the "2-line display mode" hereinafter).

When comment screen switch 28 is in the "OFF" position, no character is displayed. When it is in the "SCROLL" position, nine lines of characters with 10 characters in each line are displayed in range 22 encircled by the double-dot dash line on screen 29 of monitor TV 21 (this display mode is referred to as the "scroll display mode" hereinafter). The characters displayed in the 2-line display mode are not displayed in the scroll display mode.

In the following, the configuration and operation of the main parts of VTR 11 will be explained with reference to the block system diagram shown in Figure 4. In Figure 4, the same constituent parts as those shown in Figure 3 are represented by the same respective symbols. In this application example, four types of data can be recorded, and only one type of data is selected by switch SW_1. When a low-level signal is applied to the input ports represented by "SKIP", "ADDRESS", "COMMENT", and "INDEX" of microcomputer 12, the device enters the

recording modes of the aforementioned special function data, the aforementioned address data, the aforementioned character data, and the index signal, respectively. In this case, for example, the index signal is recorded by modulating the duty cycle of the control pulse for each bit of a digital signal, whose first bit is "0", the next 61 bits are "1", and the last bit is "0". This is different from the aforementioned address data with the signal format shown in Figure 1(A) recorded periodically. It is recorded at any time as desired by the user and is used for relative cueing playback. Consequently, a low-priced normal VTR can also have a circuit that records and reproduces the index signal.

In the recording mode, depending on the signal sent from switch SW_1, microcomputer 12 judges the data to record and generates and outputs data in a prescribed format as shown in Figures 1(A)-(C) in accordance with the data to record from keyboard 18 or the like.

If the signal to record is identified as the index signal, microcomputer 12 immediately determines whether comment rewrite key 27 is pressed. If the signal to record is identified as the address code, after the address code formed by the digits from the character keys of keyboard 18 or operation part 16 is stored in a data memory (RAM), when it is found that the VTR is in the playback mode, the microcomputer determines whether the comment rewrite key is pressed. Said comment rewrite key 27 is pressed by the user at the time point when the user sets the VTR in the playback mode and detects the header position at a desired location for recording the data by monitoring the reproduced image on monitor TV 21.

If it is found that comment rewrite key 27 has been pressed, microcomputer 12 synchronizes the phase of the playback control pulse thereafter with a reference pulse and carries out the operation of changing the duty cycle of the control pulse one bit at a time corresponding to the format of the recorded data in reading/writing circuit 13 and continues that state until the end of the recorded data.

In the following, the data recording operation in the playback mode will be explained with reference to Figures 4 and 5(A)-(F). A magnetic tape recorded with data is accommodated in a tape cassette and is loaded into VTR 11. During normal playback, the magnetic tape is drawn out from the cassette and is loaded into a prescribed tape path that winds obliquely over a prescribed angle range on a rotary body whereon a rotary head is installed (loading state). The tape runs while it is sandwiched by a capstan and a pinch roller. During running of the tape, the control pulse reproduced by control head 34 shown in Figure 4 is used as the reference signal of the phase control system of the head servo circuit used for keeping the rotation phase of the rotary head constant or as the comparative signal of the phase control system of the capstan servo circuit used for keeping the rotation phase of the capstan constant.

In this case, as opposed to the control pulse that is a square wave during recording, the playback control pulse is reproduced in a waveform as indicated by a in Figure 5(A) that

becomes a positive pulse when the recording square wave rises and becomes a negative pulse when the recording square wave falls as a result of differential processing depending on the differential characteristic or the like of the head. However, only the positive pulses among playback control pulses a are used as the control pulses in each of the aforementioned servo circuits, while the negative pulses are not used in the servo circuits.

In this case, the recorded magnetic tape is reproduced. The positive control pulses (these pulses are known as "reference pulses" in this specification) used in the aforementioned servo circuits are supplied normally to carry out the servo operation normally. Meanwhile, in order to perform recording while varying the duty cycle of the control pulses corresponding to the recorded data, re-recording (erasure) is inhibited in the reproduction interval of the referenced pulse and a certain period before and after that. In addition, in order to erase the interval between adjacent reference pulses and re-record (rewrite) the signal such that the playback control pulses become negative, microcomputer 12 applies pulse b of one frame period shown in Figure 5(B) as a switching pulse to switch circuit 33 to turn it on only during a high level period.

Meanwhile, microcomputer 12 generates and outputs pulse c, which rises at the time point of the rising edge of pulse b and falls at the time point after the period corresponding to the value of each bit of the data to record (this period is smaller than the high level period of pulse b) as shown in Figure 5(C), from its output port RECCTL 1 to recording control circuit 31 and generates and outputs pulse d, which rises at the time point of the falling edge of pulse c and falls immediately ahead of the falling edge of pulse b so that the negative pulse of playback control pulse a can be erased as shown in Figure 5(D), from its output port RECCTL 2 to recording control circuit 31.

Pulses c and d are supplied from recording control circuit 31 to control head 34 through drive amplifier 32 and switch circuit 33, respectively. Recording current e as shown in Figure 5(E) flows to control head 34. Recording current e flows in the positive direction during the high level period of pulse c and in the negative direction during the high level period of pulse d. The current does not flow when both pulses c and d are on the low level and when switch circuit 33 is off as pulse b is on the low level.

As a result, the reference pulse of playback control pulse a is kept as is, and the negative pulse is erased by the positive or negative recording current e. Also, a negative pulse is newly recorded at the time point when recording current e changes from the positive direction to the negative direction. This operation is repeated until recording of all of the bits of the data to record is ended. When the magnetic tape recorded as described above is played back later, the playback control pulse waveform is as shown in Figure 5(F).

The playback control pulse is a period of one frame, and the position of its reference pulse is the same as the original playback position before the aforementioned data are recorded.

The duty cycle becomes a first value when 1 bit of the recorded data is "1" (for example, a value such that the pulse interval between a positive pulse and a negative pulse becomes 27.5% of one frame) and becomes a second value when 1 bit of the recorded data is "0" (for example, a value such that the aforementioned pulse interval becomes 60% of one frame). When no data are recorded, the duty cycle of the control pulse becomes the aforementioned second value in the same way as in the prior art. Also, the value of the same data is recorded three times repeatedly in a prescribed signal format.

When a low-level signal is applied to input port INDEX by using data select switch SW_1, the control pulses are recorded continuously a prescribed number of times with a preset short duty cycle, and the recorded pulses become the index signal.

Data are also recorded in the recording mode of the VTR. In this case, the data are recorded while the pulse width of the recorded control pulses as the square wave of one frame period is modulated corresponding to the recorded data. In this recording mode, the VTR can also record the data after comment rewrite key 27 is pressed. This can be easily achieved by changing the software of microcomputer 12.

In the following, a cueing operation based on the data written as described above will be explained. Cueing can be performed in the loading state (playback, forward/backward search) or the unloading state (fast forward, rewind). In the case of cueing, microcomputer 12 first checks whether comment on-screen switch 28 is in the "ON" position (when it is in the "ON" position, switch circuit 28a in Figure 4 is turned on). When it is in the "ON" position, the characters of the comment for performing cueing that are input from keyboard 18 (or character keys) are generated in character generator 14 and are stored in an internal memory (RAM).

The output signal of said character generator 14 is reproduced from the magnetic tape recorded by VTR 11 and is added by adder 43 to the video signal input into input terminal 44 shown in Figure 4. The result is output via output terminal 45 and is displayed on screen 29 of monitor TV 21.

Then, microcomputer 12 enters the mode of fast forwarding or rewinding VTR 11. In that mode, the recorded data are read out from the duty cycle of the control pulses reproduced from the control track and are compared with the input data stored in the memory. If these data are the same for two rounds or more, the VTR is set in the playback mode. Then, the microcomputer controls it to enter a desired playback mode.

In the following, reading the recorded data will be explained. In the aforementioned fast forward or rewind mode, since the recorded magnetic tape runs at a high speed while accommodated in the tape cassette, it is unable to reproduce the control pulses by control head 34. However, since MR head 39 is disposed to slide in a position on the backside of the recorded magnetic tape accommodated in a tape cassette during the fast forward or rewind mode and on

the backside of the control track, the control pulses are reproduced by said MR head 39 and are supplied to Schmitt trigger circuit 41 through amplifier 40 shown in Figure 4.

Schmitt trigger circuit 41 generates pulse h that, as shown in Figure 6(B), falls when the positive pulse of reproduced control pulse g shown in Figure 6(A) is input and rises when the negative pulse of the reproduced control pulse is input. The pulse h is input to microcomputer 12 through switch circuit 37 that is connected to the side of terminal UNLOAD depending on the switching signal sent from terminal 38 in the fast forward and rewind mode. On the other hand, timing generator 42 generates timing pulse i that rises at the timing of the presence of an intermediate duty cycle between the maximal duty cycle (the aforementioned second value) and the minimal duty cycle (the aforementioned first value) of reproduced control pulse g and falls at the timing of the reference pulse as shown in Figure 6(C).

After fetching the demodulated data shown in Figure 6(D) by latching said pulse h at the rising edge of said timing pulse i, microcomputer 12 formats the data by hardware or software, reads out the data to write, and outputs them through character generator 14, adder 43, and output terminal 45 as the true values when the same value repeats two or more times as to be described later. The data are displayed on monitor TV 21. Almost the same operation is carried out in the scroll display mode (in this case, switch circuit 28b shown in Figure 4 is on).

In the following, the circuit configuration and operation of the main parts of the system for reproducing the recorded control pulses according to the present invention will be explained with reference to Figure 7. In this figure, the same constituent parts as those shown in Figure 4 are represented by the same symbols, respectively. In Figure 4, it is determined by microcomputer 12 whether the reproduced data consecutively have the same value 3 times. In Figure 7, however, this is achieved by using hardware. The reproduced control pulses input to terminal 50 are supplied to timing generator 42 and also to the data input terminal of D flip-flop 51. The data are latched by rise of pulse i as shown in Figure 6(C) from timing generator 42. In this way, the reproduced data shown in Figure 6(D) are output serially from the Q output terminal of D flip-flop 51. The reproduced data are input sequentially and serially into 15-bit shift register 52 and 64-bit shift register 53. The shift clock CK of shift registers 52 and 53 uses the clock supplied from timing generator 42 and its phase is synchronized with the reference pulse.

When the most significant 11 bits among the 15-bit data temporarily stored in 15-bit shift register 52 become the aforementioned header, the header with the known 11-bit fixed pattern is detected by header detecting circuit 54. The detected signal is applied as a latch pulse to latch circuits 57, 58, 59 through AND circuit 56. Also, the least significant four bits among the 15-bit data temporarily stored in 15-bit shift register 52 are supplied to identification signal detecting

circuit 55. Identification signal detecting circuit 55 outputs a high-level signal only when the value of the 4-bit input signal has hexadecimal value "A" and outputs low-level signal otherwise.

After latch circuit 57 latches the output signal of identification signal detecting circuit 55 when a header is detected by header detecting circuit 54, the 4-bit identification signal or data set immediately after the header is latched into latch circuit 57. Consequently, if the reproduced data are the aforementioned character data, a high-level signal is output from latch circuit 57. If the reproduced data are the address data or special function data, a low-level signal is output from the latch circuit. The output signal is output as a flag to output terminal 78 and is also applied as a select signal to each of data selectors 64, 65, 71, 72, and 75.

On the other hand, the 64-bit data output in parallel from 64-bit shift register 53 are supplied to latch circuit 58. The least significant 16 bits are supplied in parallel to comparators 60 and 62, and the most significant 48 bits are supplied in parallel to comparators 61 and 63. After latch circuit 58 supplies the latch pulse synchronized with the clock immediately after the time point when the header is detected as described above, the 64-bit data that arrived immediately before the time point when the header is detected by header detecting circuit 54 are latched into latch circuit 58 at the time point when the aforementioned latch pulse arrives. Also, the 64-bit parallel output data are supplied from latch circuit 58 and are latched by latch circuit 59 at the time point when the latch pulse is input from AND circuit 56.

Consequently, at the time point when the first header is detected by header detecting circuit 54, the 64-bit data immediately before the first header detected are temporarily stored in 64-bit shift register 53. The 64-bit data immediately before the second header that has arrived one header ahead of (past) the first header are temporarily stored in latch circuit 58. The 64-bit data immediately before the third header that has arrived two headers ahead of (past) the first header are temporarily stored in latch circuit 59. From that state, the content stored in 64-bit shift register 53 is immediately transferred to latch circuit 58 in synchronization with clock CK, and the content stored in latch circuit 58 is transferred to latch circuit 59.

On the other hand, the output signals of comparators 60 and 62 are supplied to comparators 61 and 63. Consequently, comparators 60 and 61 check whether the 16-bit and 64-bit data immediately before the second header detected one header ahead of the first header detected by header detecting circuit 54 are consistent with the least significant 16-bit data in the parallel output 64-bit data of 64-bit shift register 53 and the entire 64-bit data. Also, comparators 62 and 63 check whether the 16-bit and 64-bit data immediately before the third header detected two headers ahead of the first header are consistent with the least significant 16-bit data in the parallel output 64-bit data of 64-bit shift register 53 and the entire 64-bit data.

Comparators 60-63 output consistency signals with, for example, high level if the two input data have the same value. The output signals of comparators 62 and 63 are supplied to data

selector 64. When the select signal sent from latch circuit 57 has high level, the output signal of comparator 63 is selected and output. When the select signal has low level, the output signal of comparator 62 is selected and output. Also, when the aforementioned select signal has high level, data selector 65 selects and outputs the output signal of comparator 61. When the select signal has low level, the output signal of comparator 60 is selected and output. In other words, during reproduction of address data or special function data, the output signals of comparators 60, 62 indicating consistency/inconsistency of the 16-bit data immediately before the header are selected and output. On the other hand, during reproduction of character data, the output signals of comparators 61, 63 indicating consistency/inconsistency of the 64-bit data and identification signal immediately before the header are selected and output.

The output signals of data selectors 64 and 65 are provided to exclusive OR circuit 66. If three consecutively reproduced data are all equal to each other (consistency signals are output from both comparators 64 and 65) or are each unequal, the low-level signal is selected and output. If two out of the three consecutively reproduced data are equal to each other, the high-level signal is output. The output signal of exclusive OR circuit 66 is supplied to the J terminal of J-K flip-flop 67, and the signal output from data selector 72 is provided to the K terminal. The signal output from its Q output terminal is provided to AND circuit 73, the load terminal of counter 68, and the clear terminals of counters 69 and 70. A pulse that becomes high level at the time point when a clock pulse CK has arrived immediately after the time point when the J terminal becomes high level is output from the Q output terminal of J-K flip-flop 67.

When the output signal of exclusive OR circuit 66 has low level, counters 68-70 do not operate. When the output signal has high level, the clock pulses CK are counted. Whenever counter 68 counts clock pulse CK six times, the signal at that time is supplied to data selector 71 and counter 69. Whenever counter 69 counts clock pulse CK nine times, a signal with a prescribed level is supplied to data selector 72. Also, whenever counter 70 counts clock pulse CK seven times, a signal with a prescribed level is output to output selectors 71 and 72.

Based on the output signal of latch circuit 57, data selectors 71 and 72 selectively output the output signals of counters 68 and 769 during reproduction of the character data and selectively output the output signal of counter 70 during reproduction of special function data or address data. The output signal of data selector 71 is output to output terminal 77 through OR circuit 74 after its logical product with the Q output signal of J-K flip-flop 67 is calculated by AND circuit 73. In this way, during reproduction of character data, read clock CKO is output at output terminal 77 at a rate of once every six shifts by shift registers 52, 53. During reproduction of the special function data or the address data, the read clock is output at a rate of once every eight shifts.

On the other hand, data selector 75 outputs the 6-bit data from the earliest stored 64th bit (the most significant bit) to the 59th bit in the output signal of the 64-bit shift register 53 to output terminals 76_1-76_6 during reproduction of character data. During reproduction of special function data or address data, the data selector outputs the 8-bit data as half of the 16-bit data from the 16th bit to the 9th bit in the output signal of 64-bit shift register 53 to output terminals 76_1-76_8.

As described above, when the first two data items out of three consecutively reproduced data are the same, a consistency signal is output from data selector 65. If the first data item is the same as the third data item, a consistency signal is output from data selector 64. In either case, the read clock is output to output terminal 77. On the other hand, if the three data items are the same or none of the three data items are the same, no read clock is output. If the three data are all the same, a read clock has been output previously. Even if dropout occurs, the influence of the dropout can be alleviated significantly, and correct data output can be obtained.

In the following, an example of the operation of the microcomputer, to which the reproduced data output from said output terminals 76_1-76_8 and the read clock and the flag pulse provided from output terminals 77, 78 are provided, will be explained with reference to the flow chart shown in Figure 8. The flow chart in Figure 8 shows the processing operation during reproduction of special function data. The microcomputer receives the data obtained as described above (step S_1). The header and the data of the input special function data are separated (step S_2). The 4-bit data item immediately after the header is separated, and whether it has the hexadecimal value "B" is checked (steps S_3, S_4).

As described above, the value of the identification signal is "B" if the data are special function data. Therefore, at the time point when value "B" is detected, the microcomputer checks whether the value of the 16-bit data item after the header is "B001" or "B002" (steps S_5, S_6 [sic; S_5, S_7]). If the value is "B001", as shown in the aforementioned table, "Start of skip" is displayed. Then, the microcomputer outputs a control signal that performs an FF search (high-speed fast forward search) in the VTR on another microcomputer (known as a mechanical controller) for mechanical control of the VTR (step S_6). On the other hand, if the value is "B002", "End of skip" is displayed. Then, a control signal that switches the VTR to the play mode is output to the aforementioned mechanical controller (step S_8).

Effect of the invention

As described above, according to the present invention, in spite of a low bit rate, various kinds of data of many types (almost the same types as the SMPTE time code with a high bit rate), such as any comment (character) information, address information, and special function information, can be recorded as data, including detailed contents, very effectively and easily on

the same control track. It is possible to realize a VTR that can be used in a variety of ways even if it is an inexpensive VTR, such as a VTR used in a normal household. Also, since an identification signal is recorded, it is possible to immediately identify the type of reproduced data. In this way, the device can be immediately transferred to the next processing corresponding to the type of reproduced data. Consequently, the circuit scale can be reduced, and the software can also be simplified.

Also, during access depending on certain information data, for example, during access depending on address data, if the data are not of the corresponding type, the data will not be read out one by one. Only the same address data can be compared and accessed. The processing can be carried out very simply, and processing of different types of data is avoided. Therefore, the microcomputer can be used for other processing during that time, and the processibility of the microcomputer can be fully displayed. In addition, when the identification signal is recorded immediately before and after the header, the type of reproduced data can be identified depending on the identification signal during fast forwarding and rewinding. This is particularly suitable for data having a big block length, such as character data. In addition, since the header can be reproduced in the same pattern not only during forward reproduction of the magnetic tape but also in backward reproduction, the data can be detected quickly with a simple circuit configuration.

Brief description of the figures

Figure 1 is a diagram illustrating various application examples of the signal format of the data recorded by the method of the present invention. Figure 2 is a diagram illustrating an application example of the recording pattern of the control track recorded by the present invention. Figure 3 is a diagram illustrating an example of the overall configuration of a recording/reproducing device used for realizing the present invention. Figure 4 is a block system diagram illustrating an example of the main parts in Figure 3. Figures 5 and 6 are signal waveform diagrams explaining the operation of the block system shown in Figure 4. Figure 7 is a circuit system diagram illustrating an application example of the main parts of the system for reproducing the data recorded by the method of the present invention. Figure 8 is a flow chart illustrating an application example of the processing operation during data reproduction of the present invention.

1-1 to 1-3, 3-1 to 3-2, 5-1 to 5-4, 80	Header
2-1 to 2-3	Address information data
4-1 to 4-3, 6-1 to 6-4	Identification signal
7-1 to 7-3	Special function information data

11	VTR
12	One-chip microcomputer (microcomputer)
13	Reading/writing circuit
14	Character generator
16	Operation part for data recording/reproducing
18	Keyboard
21	Monitor TV
34	Control head
50	Reproduction control pulse input terminal

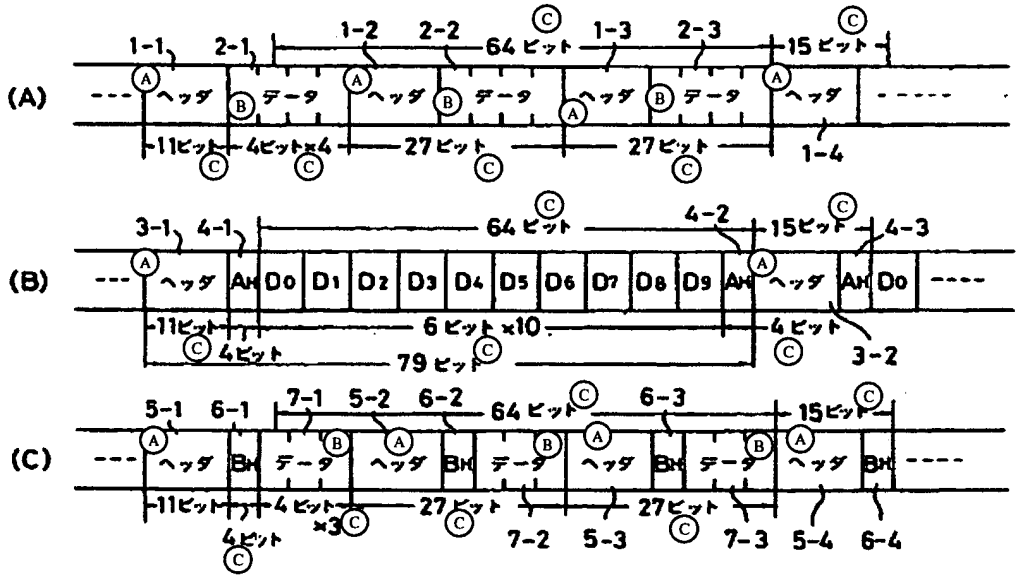

Figure 1

Key:
- A Header
- B Data
- C Bit

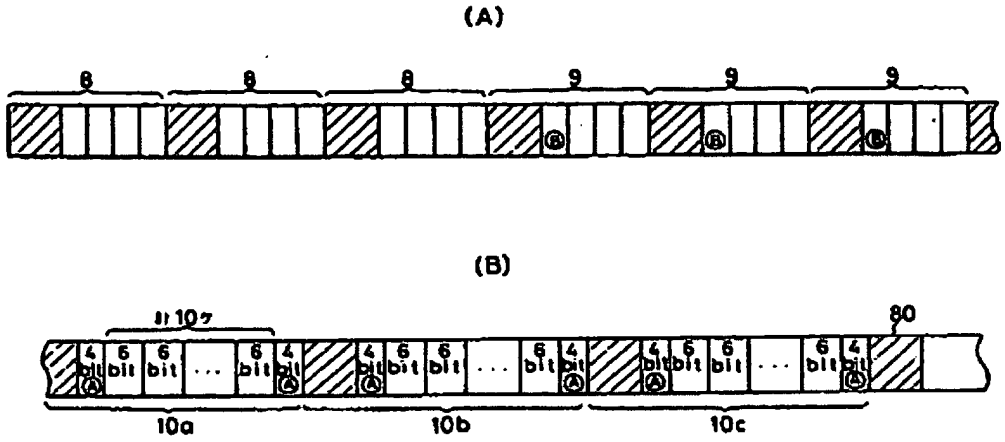

Figure 2

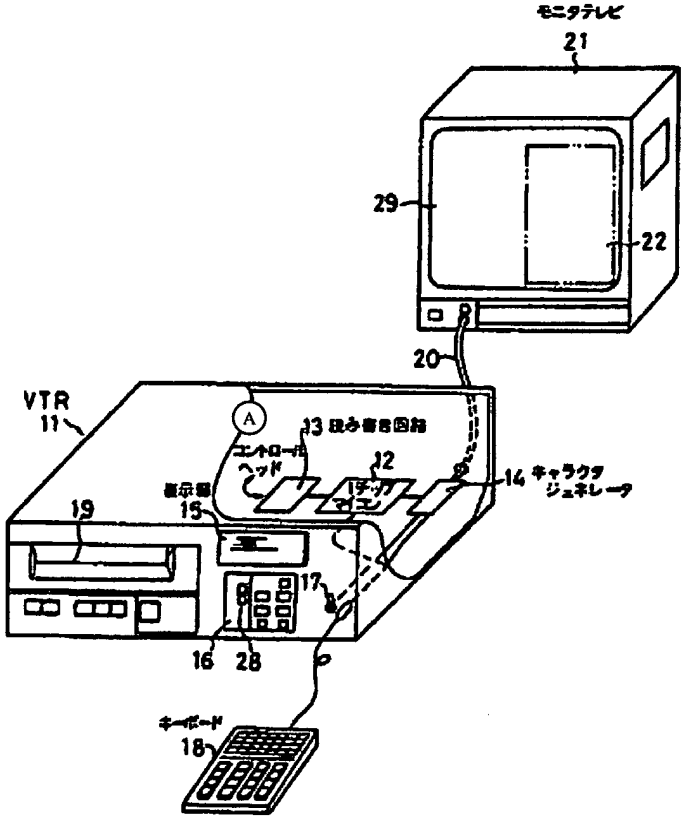

Figure 3

Key:

	A	Control head
	12	One-chip microcomputer
	13	Reading/writing circuit
	14	Character generator
	15	Display part
	18	Keyboard
	21	Monitor TV

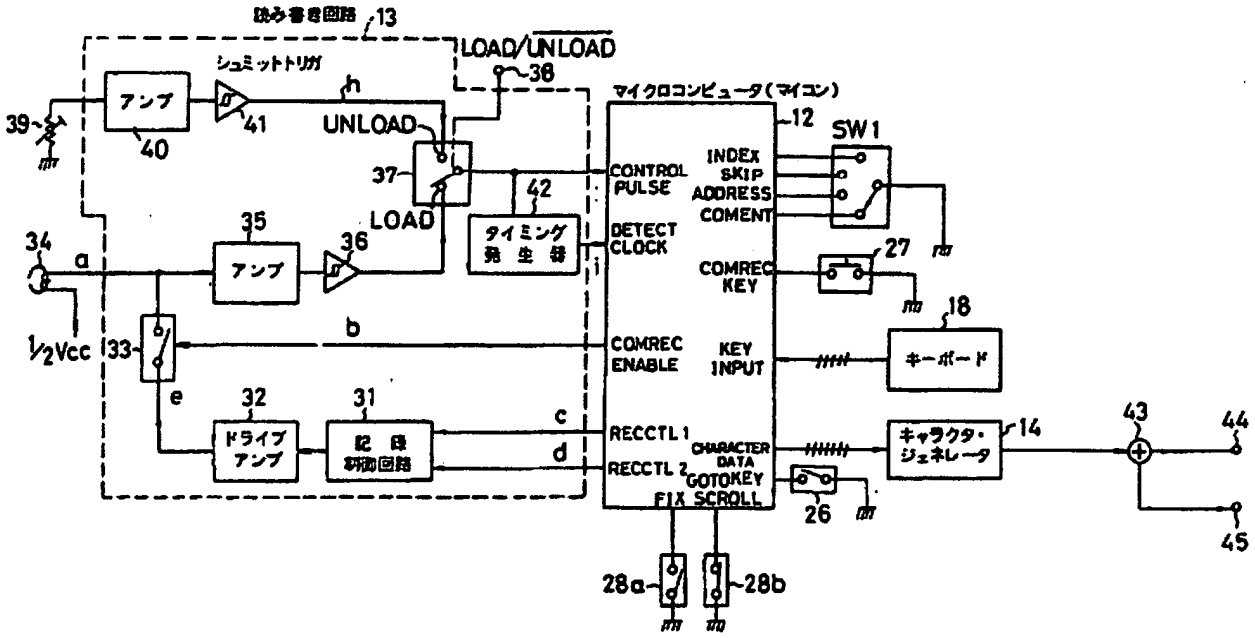

Figure 4

Key:
12	Microcomputer (microcomputer)
13	Reading/writing circuit
14	Character generator
18	Keyboard
31	Recording control circuit
32	Drive amplifier
35	Amplifier
40	Amplifier
41	Schmitt trigger
42	Timing generator

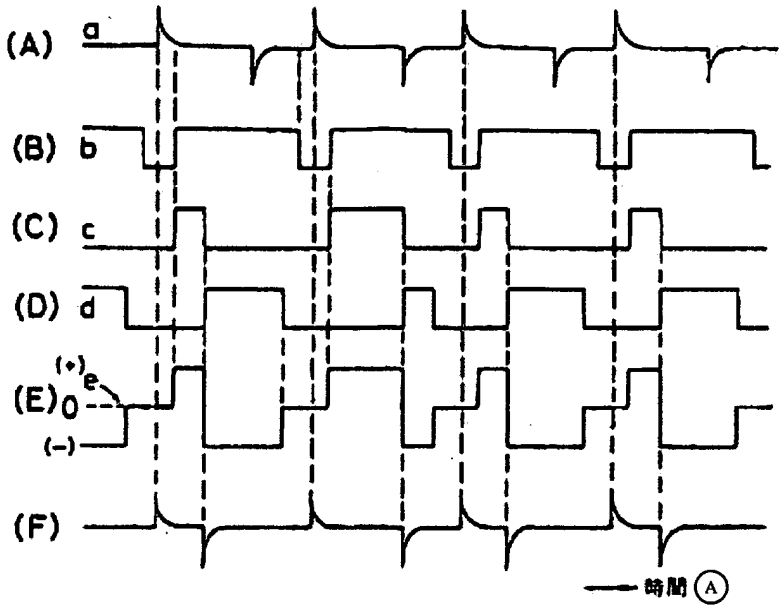

Figure 5

Key: A Time

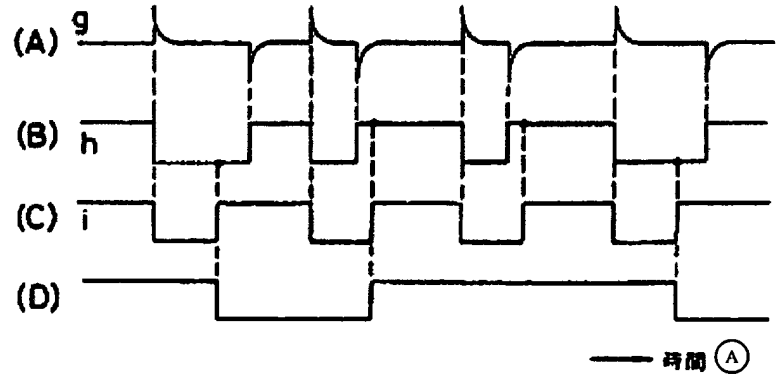

Figure 6

Key: A Time

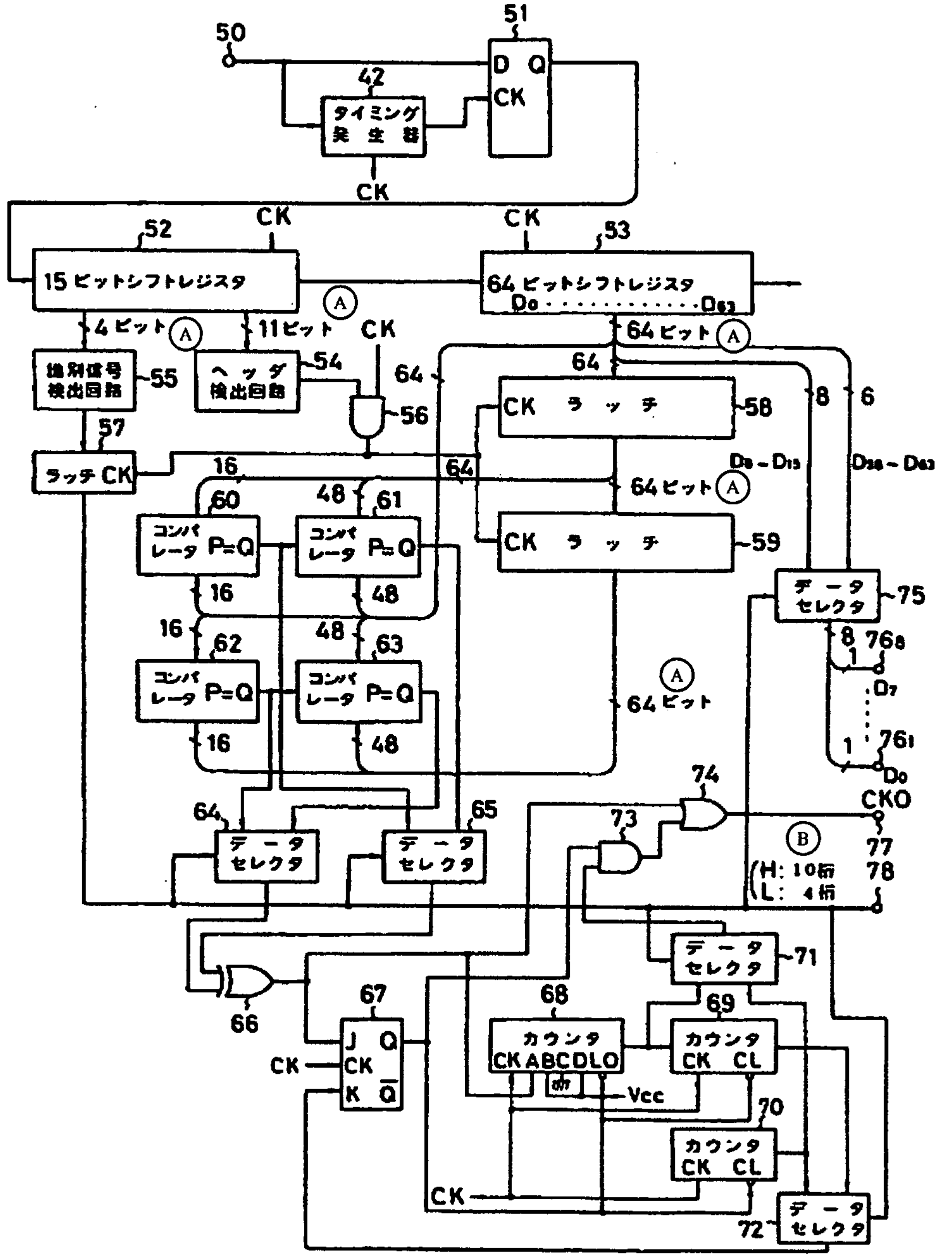

Figure 7

Key:	A	__ bits
	B	H: 10 digits L: 4 digits
	42	Timing generator
	52	15-bit shift register
	53	64-bit shift register
	54	Header detecting circuit
	55	Identification signal detecting circuit
	57	Latch CK

58, 59	CK latch
60, 61, 62, 63	Comparator
64, 65, 71, 72, 75	Data selector
68, 69, 70	Counter __

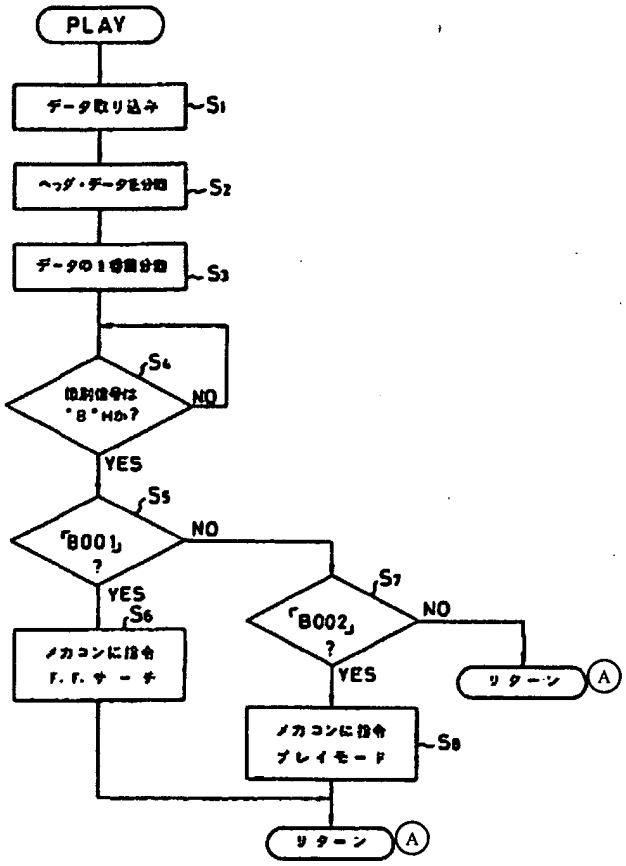

Figure 8

Key:
- A Return
- S_1 Input data
- S_2 Separate the header from the data
- S_3 First separation of the data
- S_4 Is the identification signal "B"?
- S_6 F.F. search command to the mechanical controller
- S_8 Play mode command to the mechanical controller